ABSTRACT OF THE DISCLOSURE

For a verify operation using potential Vbi', the data of a memory cell is preliminarily read by using potential Vai+1 and the state of the memory cell is stored in a latch circuit. Then, a verify/read operation is conducted by using potential Vbi'. If the state of the cell is higher than Ai+1, the outcome of the verify/read operation is forcibly brought down to a low level. Thus, only two latch circuits are required for storing an n-bit data, including one for storing the data to be written and one for preliminarily reading if the state of the cell is higher than Ai+1 or not and storing the outcome of the preliminary reading.

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